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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/383,331	08/26/1999	AMMAR DERRAA	100.718.422	6442

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EXAMINER	
SANTIAGO, MARICELI	
ART UNIT	**PAPER NUMBER**
2879	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/383,331	DERRAA, AMMAR	
	Examiner	Art Unit	
	Mariceli Santiago	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *10-16 and 25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,17-24 and 26-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The Amendment, filed on April 29, 2004, has been entered and acknowledged by the Examiner.

Claims 1-31 are pending in the instant application, claims 10-16 and 25 are withdrawn from consideration as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 5, 7-9, 17, 18, 20, 21, 23, 24, 26, 27 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeng et al. (US 5,772,485).

Regarding claims 1, 2, 4, 5 and 8, Jeng discloses a method of making a cathode assembly of an FED, comprising providing a substrate (18), made of glass (Column 4, lines 3-4), forming an emitter electrode structure (16), made of conductive material, on the substrate (18), forming a resistive layer (17), comprised of silicon (Column 4, lines 2-4), over the emitter electrode structure, forming an insulative layer (20c), comprised of silicon dioxide (Column 5, lines 41-51), on a portion of the resistive layer (17), forming at least one micropoint emitter (14)

in contact with the resistive layer (17), forming a conductive grid structure (22) spaced from the at least one micropoint (14), and forming a dielectric structure (20a) spaced from the at least one micropoint (14) and between the insulative layer (20a) and the grid structure (22).

Regarding claim 7, Jeng discloses a method wherein the insulative layer comprises a strip having a thickness of about 1000 Å (Column 5, lines 41-51).

Regarding claim 9, Jeng discloses a method wherein forming the conductive grid structure and the dielectric structure comprise depositing a dielectric layer over the insulative layer and the at least one microemitter, depositing a conductive layer over the dielectric layer, and selectively etching openings through the conductive and dielectric layers to expose the at least one micropoint emitter, with walls defining the openings being spaced away from at least one micropoint emitter (Column 6, lines 5-21).

Regarding claims 17, 18, 20 and 21, Jeng discloses a method of making A FED comprising forming a conductive structure (18), made of conductive material, forming a resistive layer (17), comprised of silicon (Column 4, lines 2-4), on the conductive structure (18), and forming an insulative layer (20c), comprised of silicon oxide (Column 5, lines 41-51), partly covering the resistive layer (17).

Regarding claim 23, Jeng discloses a method wherein the insulative layer comprises a strip having a thickness of about 1000 Å (Column 5, lines 41-51).

Regarding claim 24, Jeng discloses a method of making A FED comprising making a cathode assembly, making an anode assembly, and assembling the cathode and anode assemblies, wherein the step of making a cathode assembly includes forming an insulating layer (20c) on a portion of a resistive layer (17) on column lines forming part of an addressing matrix (Column 4, lines 12-17).

Regarding claim 26, 27 and 30, Jeng discloses a method of making an FED, comprising making a cathode assembly, making an anode assembly, and assembling the cathode and anode assemblies, wherein the step of making a cathode assembly comprises providing a substrate (18), made of glass (Column 4, lines 3-4), forming an emitter electrode structure (16), made of conductive material, on the substrate (18), forming a resistive layer (17), comprised of silicon (Column 4, lines 2-4), over the emitter electrode structure, forming an insulative layer (20c), comprised of silicon dioxide (Column 5, lines 41-51), on a portion of the resistive layer (17), forming at least one micropoint emitter (14) in contact with the resistive layer (17), forming a conductive grid structure (22) spaced from the at least one micropoint (14), and forming a dielectric structure (20a) spaced from the at least one micropoint (14) and between the insulative layer (20a) and the grid structure (22).

Claims 1, 2, 4, 5, 8, 17, 18, 20, 21, 24, 26, 27 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Moradi et al. (US 6,015,323).

Regarding claims 1, 2, 4, 5 and 8, Moradi discloses a method of making a cathode assembly of an FED, comprising providing a substrate (42), made of glass (Table 1), forming an emitter electrode structure (44), comprised of metal (ITO, Table 1), on the substrate (42), forming a resistive layer (46), comprised of silicon (Table 1), over the emitter electrode structure, forming an insulative layer (50), comprised of silicon oxide (Table 1), on a portion of the resistive layer (46), forming at least one micropoint emitter (48) in contact with the resistive layer (46), forming a conductive grid structure (54) spaced from the at least one micropoint (48), and forming a dielectric structure (52, silicon nitride) spaced from the at least one micropoint (48) and between the insulative layer (50) and the grid structure (54).

Regarding claims 17, 18, 20 and 21, Moradi discloses a method of making A FED comprising forming a conductive structure (44), comprised of metal (Table 1), forming a resistive layer (46), comprised of silicon (Table 1), on the conductive structure (44), and forming an insulative layer (50), comprised of silicon oxide (Table 1), partly covering the resistive layer (46).

Regarding claim 24, Moradi discloses a method of making A FED comprising making a cathode assembly, making an anode assembly, and assembling the cathode and anode assemblies, wherein the step of making a cathode assembly includes forming an insulating layer (50) on a portion of a resistive layer (46) on column lines forming part of an addressing matrix.

Regarding claim 26, 27 and 30, Moradi discloses a method of making an FED, comprising making a cathode assembly, making an anode assembly, and assembling the cathode and anode assemblies, wherein the step of making a cathode assembly comprises providing a substrate (42), made of glass (Table 1), forming an emitter electrode structure (44), comprised of metal (ITO, Table 1), on the substrate (42), forming a resistive layer (46), comprised of silicon (Table 1), over the emitter electrode structure, forming an insulative layer (50), comprised of silicon oxide (Table 1), on a portion of the resistive layer (46), forming at least one micropoint emitter (48) in contact with the resistive layer (46), forming a conductive grid structure (54) spaced from the at least one micropoint (48), and forming a dielectric structure (52, silicon nitride) spaced from the at least one micropoint (48) and between the insulative layer (50) and the grid structure (54).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 19, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng et al. (US 5,772,485) in view of Raina et al. (US 6,211,608).

Regarding claims 3, 19, 28, Jeng discloses a method comprising an emitter electrode structure, Jeng fails to disclose the emitter electrode structure comprising aluminum. However, in the same field of endeavor, Raina discloses a method of manufacturing a cathode assembly for an FED in which an emitter electrode structure comprises aluminum (Column 6, lines 15-17) as a suitable conductive metal material for electrode structures in FED's. It has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. Thus, it would have been obvious to one having ordinary skills in the art at the time the invention was made to have incorporate an aluminum material emitter structure in the method of Jeng, since the selection of known materials for a known purpose is within the skill of the art as evidenced by Raina's teaching.

Regarding claim 29, Jeng fails to disclose the limitation of the aluminum strips having a thickness of about 1000 Å. However, the Examiner notes that to further select a thickness of the conductor based upon the current carrying requirements of the device and known properties of the conductor would have been obvious to one of ordinary skill in the art since the same involves routine production start up procedure. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the aluminum strips having a thickness of about 1000 Å, in order to select a thickness of the conductor based upon the current carrying requirements of the device and known properties of the conductor.

Claims 6, 22 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng et al. (US 5,772,485) in view of Huang (US 5,578,896).

Regarding claims 6, 22 and 31, Jeng discloses a method as claimed, however, is silent in regards to the limitation of the insulative layer comprising silicon nitride. In the same field of endeavor, Huang discloses a method of manufacturing a cathode assembly for an FED, and further the equivalence and suitability of either silicon oxide or silicon nitride are standard materials for the insulative layer of a field emission display (Column 3, lines 9-20). It has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. Thus, it would have been obvious to one having ordinary skills in the art at the time the invention was made to have incorporate silicon nitride as an insulative layer in the method of Jeng, since the selection of known materials for a known purpose is within the skill of the art as evidenced by Huang's teaching.

Response to Arguments

Applicant's arguments with respect to claims 1-9, 17-24 and 26-31 have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mariceli Santiago whose telephone number is (571) 272-2464. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

6/14/04

Maricéli Santiago
Patent Examiner
Art Unit 2879